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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,951	06/27/2003	Roderick Holley II	2324-320	3046

64842 7590 08/04/2009

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EXAMINER	
SELLERS, DANIEL R	

ART UNIT	PAPER NUMBER
2614	

MAIL DATE	DELIVERY MODE
08/04/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/607,951	HOLLEY, RODERICK	
	Examiner	Art Unit	
	DANIEL R. SELLERS	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-26 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. **Claims 1, 3, 5, 15, 16, 18, and 26** are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et al. (hereinafter Smith), US 7,471,988 B2, in view of Beal et al. (hereinafter Beal), US 6,150,837 A.

4. Regarding **claim 1**, Smith teaches an integrated circuit used in an audio playback device, where the integrated circuit comprises:

a host interface (see column 5, lines 45-55, figure 1, unit 32, 33, 42, and 43);
a processing module operably coupled to the host interface (see column 4, lines 36-43 and figure 1, unit 22);
a multimedia module operably coupled to the processing module (see column 4, lines 44-63 and figure 1, unit 12);
memory operably coupled to the processing module and to the multimedia module in which digital audio information is stored (see column 5, lines 31-44 and figure 1, unit 32); *and*
a filter co-processor operably coupled to the processing module and to the memory, wherein at the direction of the processing module the filter co-processor retrieves digital audio information from the memory and filters the digital audio information (see column 6, line 56 - column 7, line 6, column 7, lines 31-58, column 8, lines 11-60, and figure 1, unit 12).

Smith teaches the features as shown above. Smith teaches a combined microcontroller and digital signal processor in one integrated circuit (see column 5, lines 23-30), and in another instance Smith appears to teach plural integrated circuits as evidenced by an exemplary embodiment (see column 9, lines 51-60). Even though Smith teaches all the

features, it is not clear if the integrated circuit comprises all the above features in one unit.

Beal teaches an enhanced field programmable gate array device (FPGA) (see abstract and figure 1). Specifically, Beal teaches a plethora of circuitry configurations in a integrated circuit (see column 3, lines 5-34, column 4, lines 25-59, and figure 1, unit 10). It would have been obvious for one of ordinary skill in the art at the time of the invention to combine the teachings of Smith and Beal for the purpose of lowering costs (see Beal, column 2, lines 3-18).

5. Regarding **claim 3**, the further limitation of claim 1, the combination teaches a playback mode wherein:

the filter co-processor, at the direction of the processing module, retrieves the digital audio information from the memory, filters the digital audio information to produce filtered digital audio information and writes the filtered digital audio information to the memory (see Smith, column 7, line 31 - column 8, lines 60); *and*

the multimedia module receives the filtered digital audio information from memory and converts the filtered digital audio information to a playback format (see Smith, column 7, line 59 - column 8, line 10).

6. Regarding **claim 5**, the further limitation of claim 3, see the preceding argument with respect to claim 3. The combination of Smith and Beal teaches the features of claim 3, wherein the filter co-processor performs equalization. Specifically, Smith teaches graphic equalization (see column 8, lines 11-20).

7. Regarding **claim 15**, see the preceding argument with respect to claim 1. The combination teaches these features.

8. Regarding **claim 16**, the further limitation of claim 15, see the preceding argument with respect to claim 3. The combination teaches these features.

9. Regarding **claim 18**, the further limitation of claim 16, see the preceding argument with respect to claim 5. The combination teaches these features.

10. Regarding **claim 26**, see the preceding argument with respect to claim 1. The combination teaches these features.

11. **Claim 2** is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Smith and Beal as applied to claim 1 above, and further in view of Monroe et al. (previously cited and hereinafter Monroe), US 5,911,082 A.

12. Regarding **claim 2**, the further limitation of claim 2, see the preceding argument with respect to claim 1. The combination of Smith and Beal teaches the features of claim 1, but is silent with respect to certain specifics. In the combination, Smith teaches a filter co-processor, such as a digital signal processor (DSP). However, Smith and Beal are silent with respect to programmable registers, direct memory access, and a multiply accumulator.

Monroe teaches a filter co-processor comprising:

a plurality of programmable registers operably coupled to the processing module (see column 6, lines 35-40 and figures 1 and 3, unit 30);

a Direct Memory Access (DMA) engine operably coupled to the memory and to the plurality of programmable registers (see column 7, lines 16-41 and figures 1 and 5, unit 40);

a plurality of coefficient register files operably coupled to the DMA engine (see column 6, lines 23-45);

a plurality of sample register files operably coupled to the DMA engine (see column 6, lines 23-45);

a Multiply Accumulator (MAC) engine operably coupled to the plurality of programmable registers, the plurality of coefficient register files, and the plurality of register files (see column 5, lines 16-27); *and*

an accumulator operably coupled to the MAC engine and to the DMA engine (see column 6, lines 58-60, column 7, lines 1-4, figure 1, unit 42 and figure 4, units 42 and 88).

It would have been obvious for one of ordinary skill in the art at the time of the invention to combine the teachings of Smith, Beal, and Monroe for the purpose of using a well-known DSP such as the Motorola DSP 96002 (see column 6, lines 55-57 and column 7, lines 7-8).

13. **Claims 4, 13, 14, 17, 24, and 25** are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Smith and Beal as applied to claim 3 above, and further in view of Rosefield et al. (previously cited and hereinafter Rosefield), US 5,963,153 A.

14. Regarding **claim 4**, the further limitation of claim 3, the combination of Smith and Beal teaches the features of claim 3. However the combination does not teach or suggest interpolation filtering.

Rosefield teaches an integrated circuit to perform sample rate conversions (see column 2, lines 23-30), and in performing these conversions, Rosefield teaches interpolation (see column 6, lines 15-17). It would have been obvious for one of ordinary skill in the art at the time of the invention to combine the teachings of Smith, Beal and Rosefield for the purpose of providing sample rate conversion in the audio playback device.

15. Regarding **claim 13**, the further limitation of claim 1, see the preceding argument with respect to claim 1. The combination of Smith and Beal teaches the features of claim 1, but does not teach or suggest a context switch operation with the features of claim 13.

Rosefield teaches an integrated circuit,

wherein in a context switch operation, the filter co-processor receives a context switch operation from the processing module, ceases its current filtering operations, and initiates differing filtering operations. (see column 6, lines 10-27 and 53-65).

16. Regarding **claim 14**, the further limitation of claim 13, see the preceding argument with respect to claim 13. The combination of Smith, Beal, and Rosefield teaches these features.

17. Regarding **claim 17**, the further limitation of claim 16, see the preceding argument with respect to claim 4. The combination teaches these features.

18. Regarding **claim 24**, the further limitation of claim 15, see the preceding argument with respect to claim 13. The combination teaches these features.

19. Regarding **claim 25**, the further limitation of claim 24, see the preceding argument with respect to claim 14. The combination teaches these features.

20. **Claims 6 and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Smith and Beal as applied to claim 3 above, and further in view of Kihara et al. (previously cited and hereinafter Kihara), US 5,524,022 A.

21. Regarding **claim 6**, the further limitation of claim 5, see the preceding argument with respect to claim 5. The combination of Smith and Beal teaches graphic equalization. The combination teaches the does not appear to teach a parallel mode.

22. Kihara also teaches graphic equalization (see column 2, lines 48-63 and column 3, lines 46-54). Specifically, Kihara teaches a parallel configurations using addition (figure 5a). It would have been obvious for one of ordinary skill in the art at the time of

the invention to combine the teachings of Smith, Beal, and Kihara for the purpose of using an equalizer that has symmetrical boost and attenuation characteristics.

23. Regarding **claim 19**, the further limitation of claim 18, see the preceding argument with respect to claim 6. The combination teaches these features.

24. **Claims 7, 8, 20, and 21** are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Smith and Beal as applied to claim 1 above, and further in view of Norris et al. (previously cited and hereinafter Norris), US 5,491,774 A.

25. Regarding **claim 7**, the further limitation of claim 1, see the preceding argument with respect to claim 1. The combination of Smith and Beal teaches the features of claim 1, but does not teach or suggest a recording mode.

Norris teaches a recording mode, wherein:

> *the multimedia module receives incoming audio information, converts the incoming audio information to incoming digital audio information, and writes the incoming digital audio information to memory* (see column 3, line 65 - see column 4, line 2 and column 4, lines 50-58); *and*
> *the filter co-processor, at the direction of the processing module, retrieves the incoming digital audio information from the memory, filters the incoming digital audio information to produce filtered incoming digital audio information and writes the filtered incoming digital audio information to the memory* (see column 5, lines 34-45, wherein the compression feature would require filtering).

It would have been obvious for one of ordinary skill in the art at the time of the invention to combine the teachings of Smith, Beal, and Norris for the purpose of recording signals in a portable audio player using a microphone.

26. Regarding **claim 8**, the further limitation of claim 7, see the preceding argument with respect to claim 7. The combination teaches compressing, or decimating, the audio signal.

27. Regarding **claim 20**, the further limitation of claim 15, see the preceding argument with respect to claim 7. The combination teaches these features.

28. Regarding **claim 21**, the further limitation of claim 20, see the preceding argument with respect to claim 8. The combination teaches these features.

29. **Claims 9-12 and 22-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Smith and Beal as applied to claim 1 above, and further in view of Nicol (previously cited), US 6,282,661 B1.

30. Regarding **claim 9**, the further limitation of claim 1, see the preceding argument with respect to claim 1. The combination of Smith and Beal teaches the features of claim 1, but does not teach the features of a clock circuitry that varies in frequency to effect filtering.

Nicol teaches a method of power reduction in integrated circuits (abstract), wherein the clock supplied to the filter co-processor is varied (see column 2, lines 24-37). It would have been obvious for one of ordinary skill in the art at the time of the invention to combine the teachings of Smith, Beal, and Nicol for the purpose of reducing power consumption.

31. Regarding **claim 10**, the further limitation of claim 9, see the preceding argument with respect to claim 9. The combination teaches varying the frequency of a clock to the filter co-processor, and Smith teaches using the same clock for both the filter co-processor and the processing module (see column 5, lines 23-30).

32. Regarding **claim 11**, the further limitation of claim 1, see the preceding argument with respect to claim 9. The combination teaches varying the supply voltage to the filter co-processor (see Nicol, column 2, lines 35-37).

33. Regarding **claim 12**, the further limitation of claim 11, see the preceding argument with respect to claim 11. The combination teaches varying the supply voltage to the processing module (obvious, see Smith, column 5, lines 23-30 in view of Nicol, column 2, lines 35-37).

34. Regarding **claim 22**, the further limitation of claim 15, see the preceding argument with respect to claim 9. The combination teaches varying the frequency supplied to the filter co-processor.

35. Regarding **claim 23**, the further limitation of claim 22, see the preceding argument with respect to claim 11. The combination teaches varying the supply voltage to the filter co-processor.

Conclusion

36. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Daberko et al. (previously cited), US 5,839,108 A, teaches an integrated circuit for a portable audio player (figure 1-3, and see column 4, lines 38-67);

Cowgill et al. (previously cited), US 6,606,281 B2, teaches a digital audio player (abstract);

Georges (previously cited), US 7,176,372 B2, teaches a digital multi-media player (abstract);

Johnson et al. (previously cited), US 2004/0252604 A1, teaches another digital audio player (abstract); and

Cheah et al., WO 03/023786 A2, the WIPO publication of the PCT corresponding to Smith et al., US 7,471,988 B2.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL R. SELLERS whose telephone number is (571)272-7528. The examiner can normally be reached on Monday to Friday, 9am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Curtis Kuntz can be reached on (571)272-7499. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Daniel R. Sellers/
Examiner, Art Unit 2614

/CURTIS KUNTZ/

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